

PATENT
Docket No.: P6D2-US**REMARKS**

Claim 37 has been amended, and claim 43 has been newly added. Claims 37-43 are pending in the application. Applicant respectfully requests reexamination and reconsideration of the application in light of the amendments and the following remarks.

Claims 37-42 have been rejected based on statutory-type double patenting in view of US Patent 5,864,946. Applicants have amended claim 37, replacing "silicon wafer" with the broader term "substrate." Claim 37 now is different in scope (i.e., it broader) than claim 1 of the '946 patent. Claim 37 of the instant application and claim 1 of the '946 patent are not drawn to identical subject matter. Accordingly, the statutory-double patenting rejection should be withdrawn.

Claims 37-42 have also been rejected based on obvious-type double patenting in view of US Patent 5,864,946. Applicants submit herewith a terminal disclaimer, which Applicants believe overcomes this obvious-type double patenting rejection.

In view of the foregoing, Applicants respectfully submit that the application is in condition for allowance. If the Examiner believes that a discussion with Applicants' attorney would be helpful, the Examiner is invited to contact the undersigned at (925) 456-3915.

Although Applicant believes that all necessary extensions of time have been requested and fees have been authorized in papers filed herewith, Applicants hereby petition the Commissioner for any extension of time deemed necessary for acceptance of this paper, and Applicants authorize the Commissioner to charge any fee due in connection with the filing of this paper to Deposit Account No. 50-0285 (order no. P6D2-US).

Respectfully submitted,

Date: February 25, 2002

By: 

N. Kenneth Burraston
Registration No. 39,923

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2140 Research Dr.
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PATENT
Docket No.: P6D2-US

Version With Markings To Show Changes Made

37. (Amended) Method of fabricating tip structures for ends of contact structures, comprising:
- depositing at least one layer of at least one conductive material on a surface of a [silicon wafer] substrate;
 - depositing a layer of masking material atop the at least one conductive layer;
 - patterning openings in the masking material;
 - depositing at least one layer of at least one conductive material into the openings; and
 - removing the masking material.

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail on February 23, 2002 in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.


Patti Crowder**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In the application of: Eldridge et al.

Application No.: 09/846,490

Filing Date: April 30, 2001

For: PROBE CARD ASSEMBLY AND KIT,
AND METHODS OF USING SAME

Examiner: C. Arbes

Group Art Unit: 3729

NOTICE OF RELATED PATENTS AND APPLICATIONSAssistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants wish to draw the Examiner's attention to the following commonly owned applications and patents (and the art cited therein), whose subject matter may be deemed related to the subject matter of the above-identified application.

US pat. appl. serial no.:	09/295,269	(P2D7-US)	filed	April 20, 1999
US pat. appl. serial no.:	10/011,335	(P6C1-US)	filed	December 5, 2001
US pat. appl. serial no.:	10/034,543	(P6C2-US)	filed	December 27, 2001
US pat. appl. serial no.:	10/034,528	(P6C3-US)	filed	December 27, 2001
US pat. appl. serial no.:	09/953,666	(P17D1-US)	filed	September 14, 2001
US pat. appl. serial no.:	09/023,859	(P47-US)	filed	February 13, 1998
US pat. no.:	6,336,269	(P3-US)	issued	January 8, 2002
US pat. no.:	5,974,662	(P6-US)	issued	November 2, 1999
US pat. no.:	6,246,247	(P6D1-US)	issued	June 12, 2001
US pat. no.:	5,864,946	(P7D6-US)	issued	February 2, 1999

Respectfully submitted,

Date: February 25, 2002By: 

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IN THE U.S. PATENT AND TRADEMARK OFFICE

Application No.: 09/846,490

Attorney Docket No.: P6D2-US

Inventor: Benjamin N. Eldridge et al.

Date Due: February 25, 2002

Title: PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Receipt is hereby acknowledged of the following:

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| <input type="checkbox"/> Patent Application (No. pgs ____) | <input checked="" type="checkbox"/> Petition for Extension of Time |
| <input type="checkbox"/> Information Disclosure Statement w/PTO 1449 | <input type="checkbox"/> Resp. to Notice to File Missing Parts |
| <input type="checkbox"/> Drawings ____ Sheets | <input checked="" type="checkbox"/> Response/Amendment |
| <input type="checkbox"/> Declaration and Power of Attorney (Copy from prior Appl.) | <input type="checkbox"/> Issue Fee Transmittal |
| <input type="checkbox"/> Assignment w/Cover Sheet | <input type="checkbox"/> Submission of Formal Drawings |
| <input type="checkbox"/> Check No., in the amount of \$ | <input type="checkbox"/> Notice of Appeal |
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IN THE U.S. PATENT AND TRADEMARK OFFICE

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